PhotoSound ADC

Legion Operation Manual, 2019-11-06

ADC256 Revision 1.0 and 1.1, ADC32 Rev1.0

This operation manual describes LEGION DAQ256, DAQ128, ADC256, ADC128 Rev1.0 and Rev1.1 1 and Flash DAQ32 and ADC32 Rev1.0 systems. Expert mode operation, hardware configurations, and programming guide with SDK source code description are covered in separate documents. Use of LEGION DAQ included in PhotoSound PAFT platforms is covered by a separate user manual. This manual might be changed without notice. Registered ADC system users will receive up to date versions of this manual as a part of support plan for their system. This manual cannot be distributed without explicit permission of PhotoSound.

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Table of Contents

LEGION hardware

Note: Review of Legion series DAQ design, hardware configurations (including probe input options and channel mapping), expert mode operation, MATLAB programming, and PAUS and PAFT system manual are separate documents supplied with the system and/or available upon request.

Parts

1. Assembled LEGION DAQ or ADC system with 128 or 256 channels, includes
    a. LEGION ADC256 board
    b. One (256-ch) or two (128-ch) LEGION AMP128 for DAQ or custom breakout board(s) for ADC. Note that custom breakout board might be not supplied with some ADC configuration.
    c. Ventilated housing with 2 fans installed inside.
2. AC-DC power supply (country specific model) 12V 5A output.
3. USB3 cable.
4. HDMI cable for each slave board (multi-board configurations only).
5. USB dongle with drivers and software.
6. Storage and shipping box.

Notes:

- ADC256 is based on a new Texas Instruments AFE5832 chip released in August 2017. AFE5832 is a 32-channel analog frontend chip (AFE) for Ultrasound Applications. ADC256 has eight AFE5832 chips. AFE5832 has integrated programmable amplifiers and ADCs inside. Analog part of AFE5832 consists of two dies (odd and even) 16-channels each. ADC is 16-channel with multiplexer, i.e. each ADC channel is shared between two analog channels using multiplexer. ADC clock rate is 80 MHz for Rev1.1 and Rev1.0 with latest firmware. The sampling rate for each channel is twice slower, 40 MSPS (mega-samples per second) accordingly. Note that clock rate frequency is measured in MHz, but sampling rate in MSPS. Brief datasheet for AFE5832 was published. Complete datasheet is a subject for selective disclosure, which can be requested on the product page (free registration required). PhotoSound encourages end users of ADC256 to request complete a AFE5832 datasheet from TI.
- ADC128 is identical to ADC256 except the number of channels and the number of AMP128 preamplifier boards which can be installed. ADC128 has the same USB3 data bandwidth, which allows twice high trigger rate with the same number of the data points compared to ADC256.
- DAQ models are identical to the matching ADC models except DAQ has AMP128 preamplifier boards installed.
- ADC are upgradable to the matching or higher DAQ models. ADC128 / DAQ128 are upgradable to ADC256 or DAQ256.
- Multiple ADC256 / DAQ256 R1.1 can run in parallel from a trigger supplied to the master ADC board (subject to limitations, including matching revisions of ADC boards).
- The housing has a probe input on top, digital and power connectors on one side, and cooling fans on another side.

System specific configuration and ordering options

Before start verify system specific hardware configuration in *Legion ADC hardware configuration XXXXX 201XXXXX.docx* file. As of 2019-01-16, this file contains important system specific information:

1. Serial number(s), firmware number, batch information, other labels.
2. ADC configuration
    a. ADC256 revision. Revision affects ADC clock rate 80 MHz for Rev1.1 and Rev1.0 with latest firmware and sampling rate 40 MSPS.
    b. Isolated trigger settings
        i. J13 and J16 jumper configuration, affects Isolated SMA trigger input impedance 50 Ω (closed, standard) or HiZ (open, optional)
        ii. Isolated interface voltage level 5V (standard) or 3.3V (possible upon request)
    c. ADC analog input impedance value 50 Ω (standard) or 400 Ω (optional) or other value in range 50 to 800 Ω (possible upon request)
    d. ADC analog input capacitors value 0.1 µF (standard for R1.1) or 0.01 µF (standard for R1.0) or other value up to 1 µF (possible upon request)
3. Installed preamplifier (LEGION DAQ) or adapter (LEGION ADC, optional)
    a. Model
    b. Gain mismatch tests results for standard versions (optional for some custom versions)
    c. System specific .MAP file name (matching installed preamplifier or adapter boards)
4. Power supply model (region specific) and power consumption test.

Notes:

a) Non-standard ADC analog input configuration must be specified before ADC batch production is started. Nonstandard values might cause extra lead time and / or customization surcharges.
b) Isolated interface voltage level might be modified for stock ADC boards or the existing LEGION systems at PhotoSound site.

Prerequisites

Prerequisites typically not included with LEGION products are:

1. PC with sufficient number of USB3.0 port(s) and Windows 10 64-bit
2. Free MATLAB 9.3 (R2017b) 64-bit runtime.
3. Probe with connector matching DAQ probe connectors or breakout board matching preamplifier connectors or cables.

Optional prerequisites are

4. Oscilloscope, 2-channel signal generator, and multimeter for testing the board with electrical trigger and verification of the external input trigger signal level.
5. Low power CW laser or laser pointer for testing optical trigger inputs without use of high power OPO pulsed laser.

Probe selection, connector, and pinout

The probe can be hot-swapped from LEGION DAQ and preamplifiers, except the systems with US (ultrasound) enabled. The channel mapping of acquired signal is described in the system specific .MAP file. MAP files are automatically loaded by data acquisition software ADC.exe/vi. Whole signal file is described in the system specific Excel file. Different sheets of this file describe probe pinout,

preamplifier (DAQ) or breakout adapter (ADC) signal path, and ADC256 signal path. Mode details on this subject is described in *Legion ADC hardware configuration and probe interface* manual.

Use well shielded probes. The “finger” test of the probe and connector shielding is described in Section 8 of *Legion ADC publication SPIE 2019* paper included in documentation package.

PC requirements

- Recommended PC configuration: recent generation of Intel i7, 16GB DDR4, latest Samsung M.2 PCIe SSD Pro series ≥ 1TB with installed heatsink.
- Minimal PC configuration: Intel i3 generation 2+, 8GB memory, SATA6 SSD.

Notes:

1. Performance tests with Intel i7-8700K CPU, 16 GB DDR4 XMP 3200 MHz, Samsung 1TB 970 Pro M.2 PCIe SSD components show CPU utilization at about 1%. Running a parallel heavy computation test with 50% CPU utilization (multithreading 7zip with Ultra settings) does not cause data loss, under conditions that there is no heavy SSD load or no SSD sharing between applications (extra SSD used for other applications).
2. CPU selection is unimportant for data acquisition. Recent i3 or Celeron CPU should be sufficient for data acquisition, but might be insufficient for data processing.
3. SSD performance, heat dissipation, and endurance ratings are critical for high speed data acquisition. SSD should have sustained recording rate 400MB/s per ADC256 board. Samsung 970 Pro M.2 PCIe 1TB SSD should be sufficient for two ADC256 boards with maximal recording rate, and up to four ADC256 boards with recording rate close to maximal. Samsung 960 Evo 256 / 250 GB M.2 PCIe SSD cannot provide sustained 400 MB/s recording rate. USB3 speed test is described in the Expert mode manual.
4. Use motherboard USB3 (blue color) or motherboard USB type-C ports with USB-C to USB3-B cable (not supplied). Recent generations of motherboards from top vendors (Gigabyte, Asus, MSI, etc.) have high performance USB3 interface.
5. If the number of integrated USB3 ports is insufficient or motherboard model is old, use Sonnet Allegro Pro USB3.0 PCIe card (discontinued) or Startech PEXUSB3S44V USB3.0 PCIe card. PCIe USB3 card should have dedicated USB chip and PCIe lane for each USB3 port. PCIe PC slot should be able to work and configured to work at full performance. For example, Startech USB3.0 PCIe card should be installed and configured as PCIe x4 slot, not PCIe x1. Geometric formfactor of motherboard slot does not guarantee the number of accessible PCIe lanes. Check CPU and motherboard limitations and BIOS configuration.
6. USB3.1 ports with some Asmedia controllers and some other non-Intel controllers are not currently supported because of hardware level bugs in Asmedia chips. Future support of Asmedia USB3.1 chips will be enabled in the future. Performance of Asmedia USB 3.1 ports is expected below Intel USB3.0 ports.
7. AMD chipsets typically have worse USB3 performance compared to Intel chipsets. AMD PCs were not tested, but should be working with ADC256 without problems.
8. Recommended USB3.0 and HDMI cables are AmazonBasics, Monoprice or other brand-names. Snap-on ferrite filters, like Fair-Rite 0431164951, 0431164951, 0431167281, 0431164181 can be snapped over USB3 and HDMI cables. Do not apply ferrites or other filters over AC cables or ground wires, because it can decrease EMI protection performance.

Absolute maximal ratings and recommended operation conditions

Power consumption

- Maximal ≤60W, 12V ≤5A, nano-fuse limited
- 7W typical with two cooling fans before firmware is loaded, each fan 0.5W.
- 36W typical ADC256 with two AMP128 boards, fully powered. 4 – 5W per AMP128 board.

Trigger input signal to SMA trigger input

- ≤ 6V to 50 Ω default input impedance setting with jumper(s) J13, J16 installed **or**
- ≤ 6V to HiZ without jumper(s) installed.
- Measure input impedance on input connectors using multimeter.
- Recommended signal is 4 – 5V, signal duty cycle 1%.

Analog signal to ADC input for powered **ADC** board (50 Ω to GND followed by AC coupling)

- Unpowered ADC256 board can tolerate input voltages < 100 mVpp or < 50 mV DC.
- ≤ 2Vpp AC in the absence inductive elements in the chain for powered ADC256. **If ADC is not powered, absolute maximal input signal is 0.1 VDC or ±0.1 Vpp.**
- ≤ 1 V DC (absolute value) with 50 Ω input impedance, limited by power dissipation of input resistors for powered ADC256.
- Recommended input signal is ≤ 500 mVpp, 0 V DC bias. Use zero bias or AC coupled preamplifier output. AMP128 output has 50 Ω resistor in series with capacitor (AC coupled output).

SMA128 Rev1.0 breakout board is equipped with bi-directional ESD diodes. The limitations for SMA128 Rev1.0 breakout boards are the same as ADC analog input limitations.

Standard LEGION AMP128 installed on LEGION **DAQ** system has 50 Ω output impedance and maximal output signal amplitude 3.3 Vpp to HiZ load, and 1.65 Vpp to 50 Ω load, which makes it fully compatible with standard ADC256 board equipped with 50 Ω input impedance.

- Standard AMP128 with 50 Ω output impedance cannot be used with custom ADC256 boards with input impedance > 50 Ω.
- Output impedance of AMP128 must match input impedance of ADC256. Custom version of AMP128 might be ordered for use with custom versions of ADC256.
- Input signal to LEGION DAQ or AMP128 must be < 4 Vpp AC and < 2 V DC under any conditions (powered or not powered).
- In practice the signal level > 10 mVpp will cause output signal distortion, and the signal level > 30 mVpp will cause output signal saturation.

Custom feedthrough boards are equipped with grass-clipping diodes (pair of antiparallel PIN diodes between signal and ground for each channel). PIN diode model could be Skyworks SMP1345-040L or Infineon BAR6302LE6327XTMA1. The limitation for these is a combination of ADC256 and grass-clipping diodes. Anti-parallel grass-clipping diodes are closed at voltage levels under 0.3 VDC in any direction or 0.6 Vpp (R > 1 kΩ), and open at voltage levels ≥ 1V or 2 Vpp (R < 10 Ω). Typical voltage applied to feedthrough board equipped with grass-clipping diodes should be ≤ 0.3 VDC or ≤ 0.6 Vpp, but occasional short voltage peaks exceeding this level can be suppressed by grass-clipping diodes.

Electrostatic discharge (ESD), EMI, and voltage level precautions

AMP128 probe inputs, SMA128 breakout board inputs and ADC256 digital outputs are protected from ESD damage, but individual unmounted PCB boards are sensitive to ESD discharge to ICs (integrated circuits) and interface connectors between ADC and preamplifier.

1. In order to avoid ESD damage
    a. Mount and unmount boards in ESD safe environment. Use anti-static mat connected to verified AC safety ground. Touch anti-static mat before touching the board. For example, use Startech M3013 Anti-Static Mat or similar connected to AC outlet safety ground verified using Power Gear 50542 3-Wire Receptacle Tester or similar.
    b. Handle boards using edges and large copper-filled areas on PCB board. Avoid touching ICs and internal connectors, unless using ground wrist wrap, like Tripp Lite P999-000 Anti-Static Wrist Strap with Grounding Wire or similar, connected to safety ground directly or through ESD mat.
2. Power all equipment, including ADC/DAQ and PC, from a single AC outlet or outlet pair using a single surge protection power strip, for example AmazonBasics 6-Outlet Surge Protector Power Strip, 790 Joule.
3. Do not use unapproved power supplied. Approved power supplies include Mean Well SGA60U12-P1J (recommended), GST60A12-P1J (recalled by PhotoSound due to EMI, but satisfies safety requirements), HEP-xxx-12A (xxx = 100, 150, 240, the best power supply in terms of EMI level). Please contact PhotoSound for approval if other power supply is going to be used with the system. Power supply should have isolated output and sufficient protection in case AC voltage outage, including AC power line transformer exposure. In order to minimize noise, test power supply effects on preamplifier and probe by moving power supply close to preamplifier and probe and observe noise level. For measurements, keep the distance between PSU, ADC board and probe ≥ 1 meter. See the section '*Probe selection, connector, and pinout*' for finger test of the probe and preamplifier connector.
4. In order to avoid high voltage damage,
    a. verify power supply voltage and current ratings.
    b. do not apply electrical trigger signal to ADC board which is not powered; power ADC board first.
    c. verify allowed maximal voltage level and input impedance for trigger inputs. ADC256 and ADC32 have 5V maximal trigger input level (3.3V optional). ADC16/32 and ADC128/256 have a jumper next to isolated trigger input. Input with open jumper has high input impedance (HiZ). Input with closed jumper cause 50 Ω input impedance. Before connecting the trigger verify both maximal allowed trigger level, input impedance setting (multimeter can be used), and source output impedance. 5V trigger level to 50 Ω from 50 Ω source corresponds to 10V to HiZ, which exceeds maximal allowed trigger level.
    d. verify correct trigger input. Do not connect trigger source to the trigger output;
    e. do not apply high voltage signal from ultrasound systems to ADC or amplifier products.

ADC connectors and indicators

ADC connector order is left-to-right with FPGA on top (Figure 1), right-to-left with AMP on top.

- Nano-fuse 5A
- J4, 12V 5A power connector, OD = 5.5 mm, ID = 2.0 – 2.1 mm, PC mount barrel connector. The center pin is +12V, the outer contact is ground.
- J6, J8, 12V fan connectors, must be connected to the housing DC fans
- LD4 (red, indicates reverse power polarity or blown fuse), LD1, LD3, LD2 (green).
- J11, USB3 B connector, connect USB3 A to B cable to PC (A-side).
- PD2, PD1 optical fiber trigger input connectors (locking type) for 2mm optical fiber.
- Isolated trigger interface #2:
    a. J17 SMA trigger out, low input impedance 5V ±10% output
    b. J15 SMA trigger in, 5V maximal input signal level, verify with oscilloscope using matching impedance settings.
    c. J16, .1" two-pin jumper; J15 input impedance is 50Ω, if closed, or HiZ if open.
- Isolated trigger interface #1:
    a. J14 SMA trigger out, low input impedance 5V ±10% output.
    b. J12 SMA trigger in, 5V maximal input signal level, verify with oscilloscope using matching impedance settings.
    c. J13, .1" two-pin jumper; J15 input impedance is 50Ω, if closed, or HiZ if open.
- J7, HDMI connector, Master output for synchronization with slave ADC256 board. Not in use on DAQ128 / ADC128. **Do not connect to PC or monitor to this connector.**
- J5, HDMI connector, Slave input for synchronization with master ADC256 board. Not in use on DAQ128 / ADC128. **Do not connect to PC or monitor to this connector.**

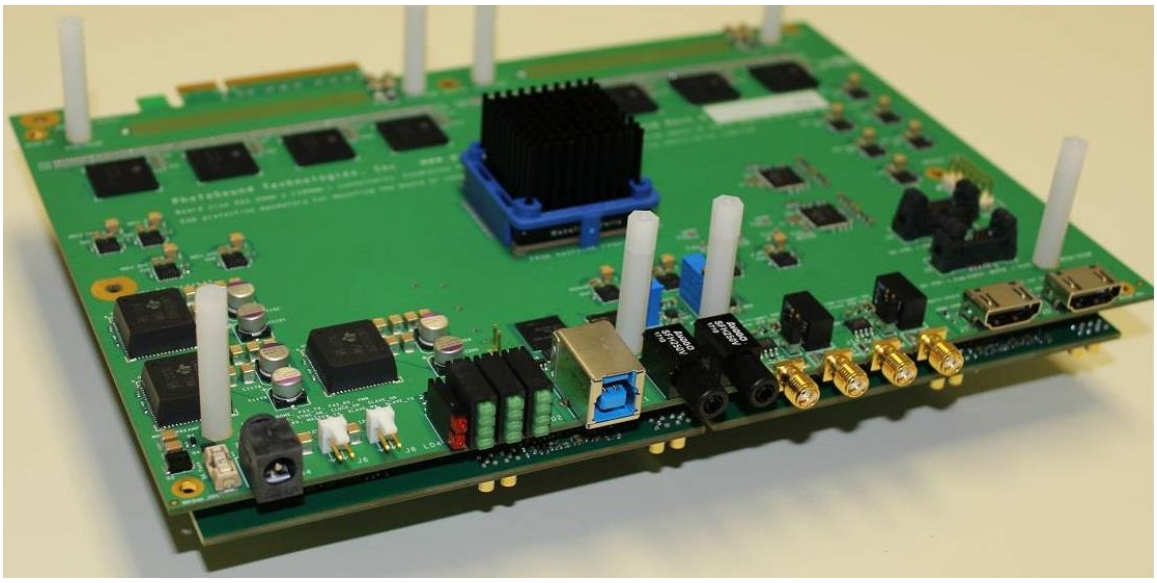

Figure 1: LEGION DAQ256 with ADC256 Rev1.0 board on top. ADC256 front components / connectors from the left-to-right are nano-fuse, power, 2x fans, 4x LEDs blocks, USB3 type-B, 2x optical fiber trigger inputs, 4x SMA trigger IO, 2x HDMI master and slave.

Figure 2: LEGION DAQ256 top (probe connector side) view. ***Note:*** *probe connector might be different. Note: MMCX test preamplifier IO connectors (not connected to ADC analog interface) might be available on some preamplifier boards. If extra test preamplifier channels are needed order Flash AMP16-18 with SMA interface and optional SMA128 breakout board for ADC256/128.*

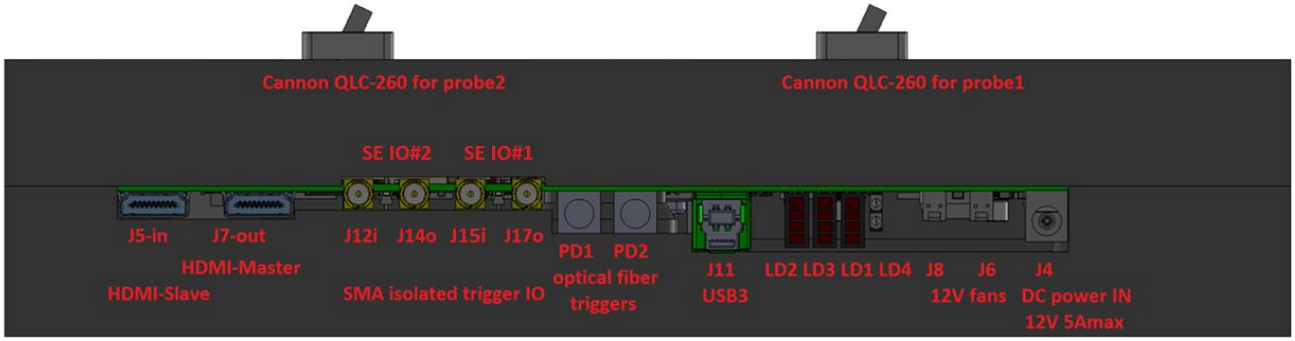

Figure 3: LEGION DAQ256 front view. LEGION AMP128 are mounted on the top, LEGION ADC256 is on the bottom with digital connectors facing to the front. Cooling fans are mounted on the right side of the housing. Fan wiring is not shown.

LED indicators

LED indicators of ADC256 shown in Figure 3 are listed starting from PCB (top to bottom) below:

LD2, green, 4-position, clock and master-slave synchronization

1. Slave_OK, indicates that board is configured as a slave board in many board configurations;
2. Clock_OK, indicates that ADC clock is running correctly;
3. Sync_OK, indicated that the slave board is synchronized with master board;
4. Init_OK, indicates that the board is initialized.

Correct indicator values after boards are completely configured by ADC.exe/vi software:

- LD2.2 and LD2.3 ON for a single board or the first master board.
- All LD2 LEDs ON for slave boards.

LD3, green, 4-position, master-slave communication:

1. Stave_TX
2. Slave_RX
3. Master_TX
4. Matser_RX

There are no specific requirements for these LEDs

LD1, green, 4-position, power, USB3, and configuration

1. Power (very dim);
2. FX3_RX, USB3 data from PC to ADC256;
3. FX3_ TX, USB3 data from ADC256 to PC;
4. CFG_DONE, configuration of ADC256.

LD1.1 is always on, if ADC 256 correctly powered. LD1.2 and LD1.3 are blinking during data transmission.

LD4, red, 2-positions, indicates critical power failures

1. Fuse, indicated blown fuse, replace fuse with 5A fast nano-fuse.
2. Power polarity, indicates wrong power polarity. Warning: reverse power polarity protection might not work, if power supply is not isolated. Always use isolated power supply. Ground the the probe or preamplifier signal ground.

All LEDs on LD4 must be OFF.

Trigger input notes:

- Trigger input source is programmatically selectable between PD1, PD2, J12, J15 or combinations. LEGION board is typically using only single trigger input. Optical trigger PD1 or PD2 are preferred trigger sources.
- If the trigger source is electric applied to SMA J12 or J15, verify input impedance setting on jumpers J13 and J16 accordingly. Input impedance can be also measured using Ohmmeter if the board is not powered.
- **The trigger applied level to SMA trigger inputs must be within 4 – 5.5 V. Verify voltage level applied to this connector using oscilloscope input with 50 Ω (closed jumper) or HiZ (open jumper) setting depending on input impedance jumper position. ATTENTION: 4 – 5 V to 50 Ω load corresponds to 8 – 10 V to HiZ load, which will irreversibly damage the isolator IC (Analog ADCMP605BCPZ). High voltage damage to trigger interface IC is not covered by warranty.** If oscilloscope does not have 50 Ω input, use 50 Ω BNC adapter, like Rigol ADP0150BNC or similar.
- Isolated trigger output SMA connectors have 5V ±10% output signal and 50 Ω output impedance. The output trigger amplitude is 5 V ±10% to HiZ load and 2.5V ±10% to 50 Ω load. The output can drive 50 Ω load with a low duty cycle and HiZ with any load cycle. Output trigger signal can be programmed using SDK.

Hardware parameters

1. ADC data rate is currently fixed at 40 MSPS for Rev1.1 and Rev1.0 with latest firmware. Each odd and even ADC channel clocks are interleaved (shifted half period with respect to each other).
2. LEGION AMP128 preamplifier base version has a high input impedance 39 kΩ. Without probe connection, DAQ256 records 39 kΩ resistor || 10 pF input capacitance thermal noise. Probe intrinsic capacitance acts as RC low pass filter for noise spectrum, which reduce high frequency noise level up to 8 dB. For example, 100 pF probe connected to 39 kΩ resistor produce -3 dB corner frequency $1/2\pi RC$ = 41 kHz. The corner frequency estimate cannot be fully trusted, because probe capacitance is separated from preamplifier input resistor by a long transmission line with open and close end reflective termination on the probe side and resistor side accordingly. Such transmission line has ¼-wavelength resonance state.
3. LEGION ADC256 has 2Vpp ADC scale, 12-bit resolution. ADC selectable gain range is 12 - 51 dB (low power mode = ON) or 6 – 45 dB, if -8 dB input attenuator enabled as needed. The maximal measurable input range is 1 Vpp at 6 dB gain. ADC full input scale with 51 dB gain is 5.6 mV (2Vpp / 51dB) and resolution is 1.4 µV (5.6 mV/4096 12-bit). ADC absolute maximal input rage is ±1 VDC or 2Vpp for brief time, if ADC is powered or 0.1 VDC or ±0.1 Vpp, if ADC is not powered.
4. LEGION DAQ with standard AMP128 40 dB (100x) preamplifier has maximal measurable input range 10 mVpp (1 Vpp / 100) at 6 dB gain. DAQ full input scale with 51 dB gain is 56 µV (2 Vpp / 91 dB) and resolution is 14 nV (56 uV/4096 12-bit). Absolute maximal input rage is ±2 VDC or 2 Vpp (does not damage equipment) for powered or unpowered DAQ.

LEGION AMP128 preamplifier gain is about 40 dB over 25 kHz to 35 MHz bandwidth (-6 dB, measured using signal generator). Preamplifier bandwidth with probe attached will be smaller. Exact gain value and HP filter characteristics depends on the probe capacitance, wiring, and measurement method. Preamplifier input has to be treated as a high impedance input. Preamplifier output is AC coupled and has 50 Ω resistor is series. Preamplifier output is designed to drive 50 Ω load with a small signal ≤ 100 mVpp. Larger output signal might be distorted.

Hardware Installation

1. LEGION DAQ must be installed indoors in ventilated environment, non-compensating humidity, and temperature range from 15 to 30°C. If DAQ was stored or transported at low temperatures let DAQ reach room temperature for 24-hours.
2. DAQ should be operated inside the housing or in ESD safe environment. Input connectors have ESD protection. Do not create any unapproved connections.
3. Connect the probe(s) to AMP128 Cannon QLC-260 connector(s).
4. Use high quality USB3 A to B cable (optional ferrites might be attached close to both connectors).
5. **Power all AC equipment, including computer, DAQ, oscilloscope, and trigger source from one AC power strip. AC power source must have safety ground.**
6. The board is powered by a single 12 VDC power supply (provided). Typical power consumption of DAQ256 is <36 W of which <26 W for ADC256 and 5 W for each AMP128. Rated power is 60 W (5 A nano-fuse installed). Use high quality isolated AC-DC power supply with 2.1 mm barrel connector (the central pin is +) rated at least 5A (60 W).
7. Note, that oscilloscope-integrated signal generators, like Siglent SDS2104X, usually have inferior signal quality compared to standalone signal generators, like Siglent SDG2042X.
8. If ADC with SMA breakout board is tested using a signal generator, for the best signal-to-noise ratio, the signal generator should be powered from UPS (battery supply) running from the battery (not connected to AC outlet!). Preamplifier input signal level should be < 10 mVpp to HiZ load. Use SMA attenuators as close as possible to preamplifier input.
9. Turn on preamplifier power programmatically. Green LED on preamplifier board indicates that preamplifier is powered.
10. The board must be used with proper ventilation: Top and bottom ground planes of ADC256 board are used as heatsinks.
11. Power the trigger source and DAQ/ADC from the same AC outlet.
12. **Apply trigger signals only after ADC board is powered. Before applying trigger signal, verify the signal level with oscilloscope as described above.**

Standard and custom preamplifier and adapter boards

DAQ256 / DAQ 128 devices are ADC256 / ADC128 devices with installed 2 or 1 AMP128-18 preamplifier boards using Samtec SEAFP-50-05.0-S-06 J9 and J10 pressfit connectors on ADC and Samtec SEAMP-50-02.0-S-06 pressfit connector on preamplifier. Analog inputs and outputs have ESD protection, which cannot protect amplifiers in case if high voltage level is applied from US machine in transmit mode. If one preamplifier board is used with ADC128 / DAQ128 install it on J10 connector.

New PhotoSound preamplifiers (2018) are based on ON Semi JFETs for the first amplification stage and opAmp as the second amplification stage and the line driver capable in driving 50 Ω load for a small signal. Previous generation of PhotoSound preamplifiers (2016) was based on NXP dual-gate MOSFET (BF908 or BF998). All NXP RF FETs were recently discontinued, most of them are not available for sale. Infineon FETs are not recommended for a new design and does not match exactly to similar NXP FET models. A design challenge was using a low-quality model JFET (supplied by manufacturer), which does not match the actual part behavior. Actual preamplifier design was tested and validated using direct measurements.

New preamplifier design is generally matching previous design in terms of gain, noise, power consumption (slightly improved), footprint (reduced). Signal to noise level for new preamplifiers is significantly better for low frequencies, matching the old design at ~ 3 MHz, and slightly inferior above 5 MHz. New preamplifier footprint is 2 mm x 22 mm per channel. Input power for opAmp and JFET 3.3 V, < 10 mA. Supply voltage before LDO can be as low as 3.6 V.

Standard preamplifier AMP128-18 with 40 dB gain has the following specs:

- Analog inputs have ESD protection, which cannot protect amplifiers in case, if high voltage level is applied from US machine in transmit mode. Preamplifier analog outputs and ADC inputs does not have ESD protection. Connect preamplifier in ESD safe environment.
- Gain 40 dB to 50 Ω load, 46 dB to highZ (high impedance), measured using signal generator and oscilloscope. Gain measured with probe depends on the probe capacitance and generally slightly lower.
- **Preamplifier is inverting** due to second opAmp stage. All other signal stages are not inverting. Multiply output signal by -1, if needed.
- Th absolute maximal output signal to 50 Ω load is 1.75 Vpp, which does not exceed absolute maximal input signal level for standard version of ADC256. Custom versions of ADC256 with increased input impedance cannot be used with standard version of AMP128-18, because the maximal output signal from standard AMP128-18 to HiZ load is 3.3 V. Custom version of AMP128-18 with output impedance matching input impedance of ADC must be used with custom version of ADC256.
- Recommended operating conditions: input signal ≤2 mVpp to highZ load, which corresponds to 200 mVpp output to 50Ω load or 400 mVpp to highZ load. 10 mVpp to highZ input is acceptable, but not recommended. Input signal level >10mVpp to 50 Ω (= 20 mVpp to highZ) input will cause preamplifier output saturation and high distortions. Under any conditions the input signal should not exceed 2Vpp (such input signal will cause preamplifier output saturation).
- Preamplifier has rail-to-rail design at 3.3 V, which means that maximal output signal is ≤3.3 Vpp to highZ load, and ≤1.65 Vpp to 50 Ω under any conditions.
- BW -6 dB 25 kHz – 35 MHz, BW -3dB 40 kHz – 30 MHz measured using signal generator.

    - Note: actual BW depends on the probe capacitance.
- Shielding, ground stitching – PCB internal:
    - Signal layers are internal; all signal layers are internal and coupled to ground.
    - Layers are ground filled; signal traces are ground stitched.
- Cross-talk < -50dB, except for custom models with Cannon DLM connectors due to 3d party pinout mistakes.
- Input impedance 39kΩ, the best in terms of noise according to tests. Custom values of input impedance available upon request.

End user can design their own preamplifier or adapter boards for use with ADC256 / ADC128. Pinout of ADC connectors is available in the channel map Excel file. The size of each AMP128-18 board is 108 mm x 160 mm x 2 mm thick. Adapter board can be 160 mm x 233.35 mm have all 256-channels. Adapter board templates are available from PhotoSound upon request. Maximal combined power, which can be supplied from ADC Rev1.0 board to preamplifier boards or adapter board is 12 W on both 3.6 V and 12 V power rails. To satisfy absolute maximal ratings for ADC256 analog input, use a pair of anti-parallel grass-clipping PIN diodes (Skyworks SMP1345-040LF or Infineon BAR6302LE6327XTMA1) between signal and ground for each analog output of your custom breakout or preamplifier board.

Low-gain preamplifier AMP128-18 version with 9 dB gain has the following specs different from 40 dB gain preamplifier:

- Single amplification stage (JFET only) preamplifier with 9 dB gain, **non-inverting**
- Designed to drive 400 Ω load and require a custom version of ADC with 400 Ω input impedance as well as matching 400 Ω config.ini settings. Use of low=gain preamplifier with a standard 50 Ω ADC will cause low amplitude signal as well as some BW distortions.
- Each preamplifier output has a pair of antiparallel PIN diodes for ADC input protection.

Signal path and filters for ADC256 / ADC128

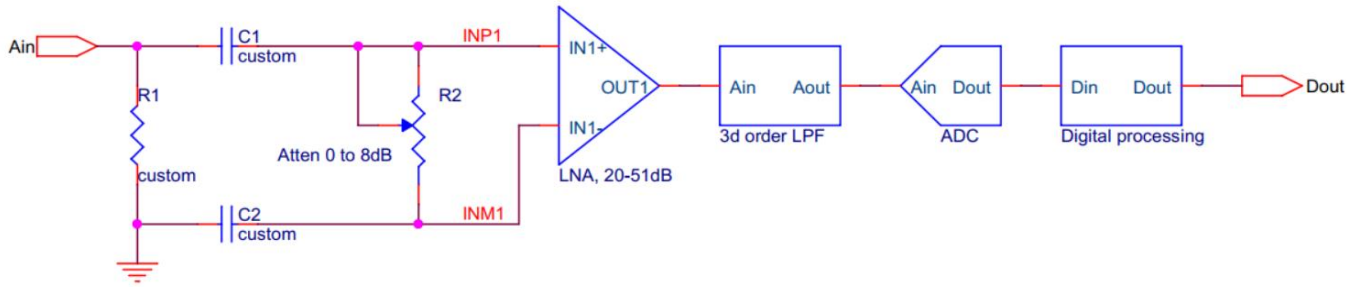

Figure 4: Signal path for one channel of ADC256. Resistor R1 and capacitors C1, C2 are discrete components soldered to ADC256 board. Value of these components can be customized. The acceptable range for R1 is from 50 Ω (default) to 800 Ω. Value for C1 and C2 is 10 nF for Rev1.0 and 0.1μF for Rev1.1. Custom boards might have capacitor value up to 1.0 μF. All other blocks, including attenuator R2 are located inside AFE5832 chip and controlled in programmable way using ADC, VCA, and DGTC registers as described above. ADC multiplexing between adjacent odd and even channels is not shown.

1. The first order analog HPF is formed by input RC chain and 0 – 8 dB attenuator. With highest attenuator setting -8 dB and default R1 and C1, C2 settings, HPF corner frequency is about 370 / 37 kHz and -6 dB point 300 / 30 kHz for Rev1.0 / Rev1.1 accordingly. Disable attenuator using check box attenuator enabled in ADC tab, Figure 17, if low frequencies are needed. **If attenuator is disabled, there is no low frequency loss at this stage. As mentioned above, the attenuator affects only gain codes 0 to 63.**
2. LNA is low-noise amplifier with programmable gain in range 20 to 51 dB in low power mode and 14 to 45 dB in high power mode. First order LPF cutoff frequency can be programmed in the range 5 to 12.5 MHz for low-power mode or 10 to 25 MHz for high-power mode (ADC tab, Figure 17). This filter can be programmed, but cannot be disabled.
3. 3d order LPF is 3d order analog low-pass filter, which can be set at 75 or 150 kHz, , Figure 17. This filter can be also disabled for all channels or some channels.
4. ADC input is analog, the output is digital. ADC is shared between odd and even channels. For example, channels 1 and 2 are sharing the same ADC operating with clock rate 80 MHz for Rev1.1 and Rev1.0 with latest firmware. Sampling for each channel is 80 MHz / 2 = 40 MSPS. Data for the channel 2 is delayed with respect of channel 1 by one ADC clock period (1 / 80 MHz).
5. Digital post-processing block is completely bypassed in low-latency mode on ADC tab, , Figure 17. Low latency mode also reduces data pipe-line delay after trigger is received by 4 ADC clocks or 2 sampling periods. Note: Each ADC clock = 80 MHz and the sampling period is 25 ns for R1.1. The data pipe-line works like a memory buffer, which cause delay of data transmission from ADC to FPGA memory, i.e. with larger delay more data acquired before the trigger event. Digital HPF filter can be used, if the low-latency mode was not enabled. Digital HPF parameters depends on the sampling rate (corner frequencies are proportional to the sampling rate), see Table 1 below. Use of digital HPF corner 10 is highly recommended for DC bias removal. *ADCs HPF output rounding* might be used to enable rounding of 14-bit ADC output after digital HPF. If *ADCs HPF output rounding* is not enabled 2 lower bits from 14-bit ADC output are dropped.

Table 1: ADCs digital HPF corner frequency vs corner code number for ADC256 operating at 40 MSPS.

HPF corner setting	HPF, kHz (at 40 MSPS)
Disabled	None
2	2780
3	1490
4	738
5	369
6	185
7	111
8	49
9	25
10	12

Advice: Disable attenuator, if possible. If lower gain is needed, use high power mode: uncheck low-power mode on VCA page.

Calculation of attenuation and HPF for attenuator: Preamplifier output impedance R_{preamp} default value is 50 Ω, the input impedance seen by attenuator is $\mathrm{R_{in}} = \mathrm{R_{preamp}} \,||\mathrm{R_1} = \frac{\mathrm{R_1 R_{preamp}}}{\mathrm{R_1 + R_{preamp}}}$. Under assumption that $C_1 = C_2$, and $R_{preamp} = R_1$, R_S should be set as $R_1/2$. In the following R_S is input resistance value set on VCA pages, $R_{in} = R_1/2$ is physical value of input impedance seen by attenuator.

$$R_{atten} = \frac{R_S}{(10^{G/20}-1)},$$

where $G = (64 - ManualGain)\ 0.125$ in dB for manual gain < 64. For manual gain ≥ 64 attenuator is and should be disabled.

If $R_{in} \neq R_s$, the actual gain is $G_{actual} = 20\log_{10}(\frac{R_{in}}{R_{atten}} + 1)$.

The attenuation frequency dependent factor is $\left(1 + \frac{2}{sC_1(R_{in}+R_a)}\right)^{-1}$, where $s = i2\pi f$.

The attenuator HPF -3 dB corner frequency is $f_c = 1/(\pi C_1(R_{atten} + R_{in}))$,

Example 1: For default configuration of DAQ256 Rev1.0, R1 and R_{preamp} = 50 Ω, C1 and C2 are 10 nF. R_{in} = 25 Ω, and R_S set on VCA pages as 50 Ω. If manual gain code was set 0, G = 8 dB (calculated), R_{atten} = 33 Ω, actual attenuation is 5 dB, and -3 dB frequency 550 kHz.

Example 2: For of DAQ256 Rev1.0, R1 and R_{preamp} = 400 Ω, C1 and C2 are 10 nF. R_{in} = 200 Ω, and R_S set on VCA pages as 200 Ω. If manual gain code was set 0, G = 8 dB (calculated), R_{atten} = 133 Ω, actual attenuation is the same as attenuation set 8 dB, and -3 dB frequency 96 kHz.

LEGION driver and software setup

ADC256 driver installation

LEGION ADC256 is equipped with FX3 USB3 chip from Cypress Semiconductor and use propitiatory FX3 Cypress driver (see release and copyright notes in the driver folder). The driver is located in *\driver* folder.

1. Connect ADC256 to PC using USB3 cable.
2. On PC open *Device manager* and expand USB devices section.
3. Power ADC256 using provided 12VDC power supply with 2.1mm barrel connector.

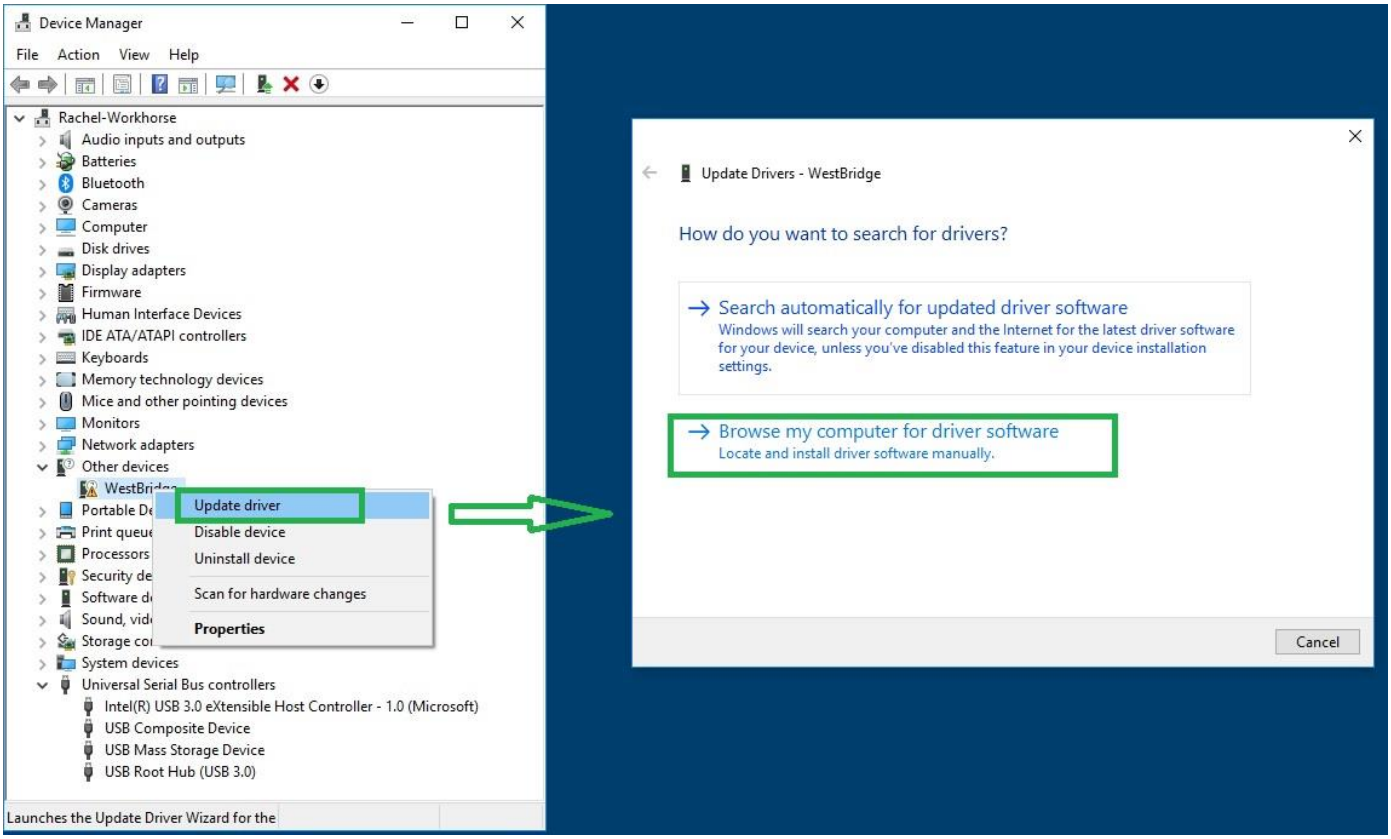

Figure 5: ADC256 driver installation. Step 1.

4. Find a new device in Device manager, Figure 5. Device will be originally recognized as *Other devices/WestBridge* with yellow triangle indicating driver error. If driver was preinstalled or another driver was found on the computer, uninstall all previously installed drivers as described in
5. RMB (click right mouse button) on *WestBridge* device and choose update driver. Next choose *Browse my computer for driver software*.
6. Follow Figure 6. Choose *Browse …, Browse For Folder* with ADC256 driver, next choose subfolder with your Windows version. Press OK. Note, that driver supports both 64-bit and 32-bit Windows, but ADC256 software supports only 64-bit versions of Windows.
7. Verify that the driver was installed as *Cypress FX3 BootLoader Device* (before firmware is loaded) which turns to *Cypress FX3 StreamerExample Device* after firmware is loaded; see Figure 7 for one board or Figure 8 for two boards.

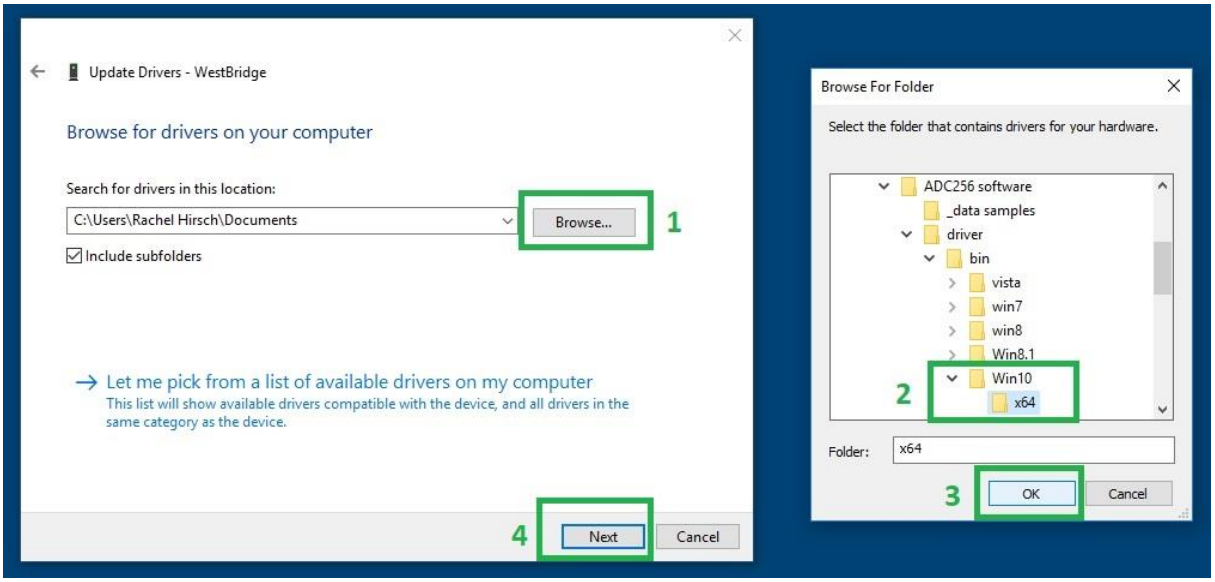

Figure 6. ADC256 driver installation. Step 2.

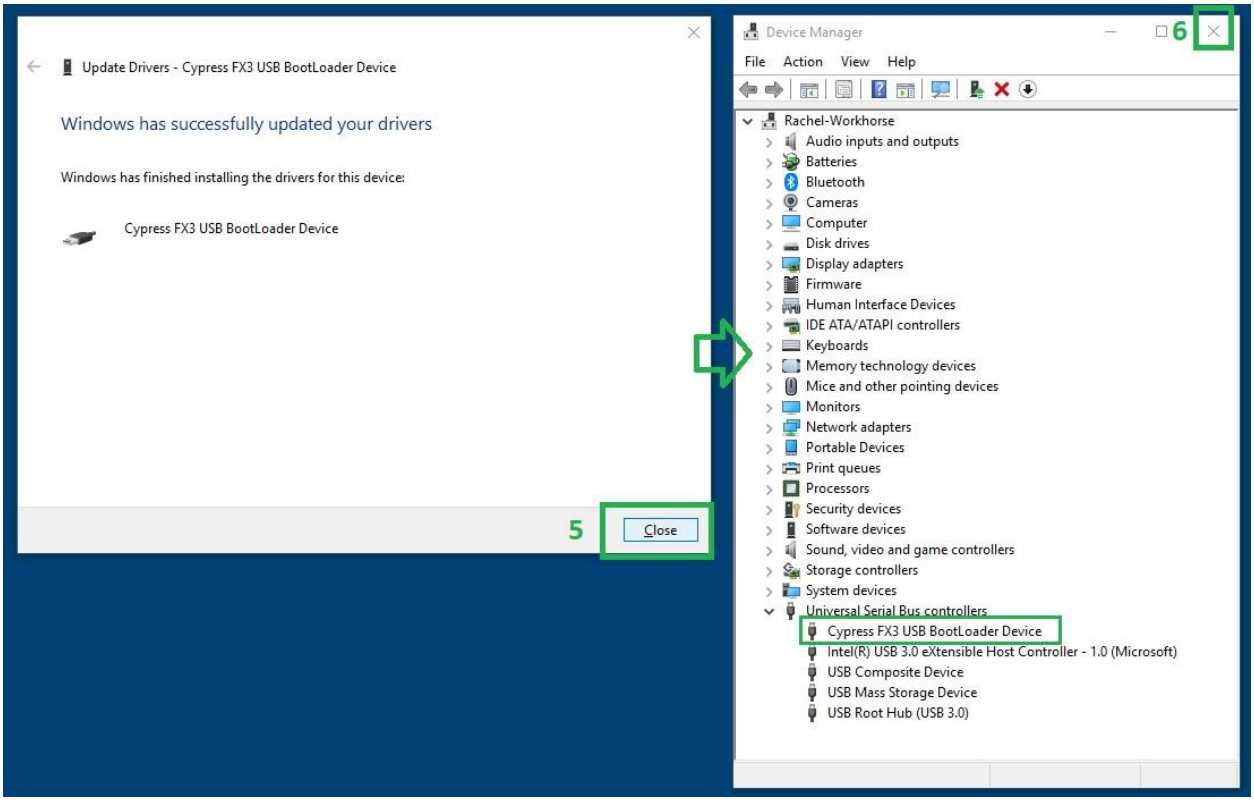

Figure 7. ADC256 driver installation. Step 3.

8. For multiple ADC256 devices or different revisions of ADC256 device connected to a single computer the driver should be installed only once, for the first ADC256 board.
9. How to uninstall incorrect ADC256 driver.
    a. If the device has multiple drivers or incorrect driver, uninstall device in the *Device Manager*: Find the device, RMB (right mouse button) click, *Uninstall*, mark *Delete the driver software for the device*, OK.
    b. Unplug and plug USB.
    c. Verify that all drivers for the device were deleted using *Device Manager*. If any driver left repeat 4a.
10. *Note*: Do not unplug USB3 cable after firmware was loaded, because ADC256 would not be recognized by Windows. After power cycle of PC, power cycle ADC256 board, but keep USB3 cable always plugged. Power cycle ADC256 board, if USB3 cable was unplugged with loaded firmware.

Figure 8: Two ADC256 boards with loaded firmware were recognized as Cypress FX3 Streamer Example Devices in Windows Device Manager.

Setting up software environment: application and SDK installation

1. Install MATLAB 2017b (9.3) Runtime for compiled version only or MATLAB 2017b for source code. Restart computer, if prompted.
2. Extract 7zip archive with application software to any folder.
3. For application software run DAQ.exe file.

LEGION software

Run *DAQ.exe* and wait until firmware is loaded to ADC128 board as described in Figure 9.

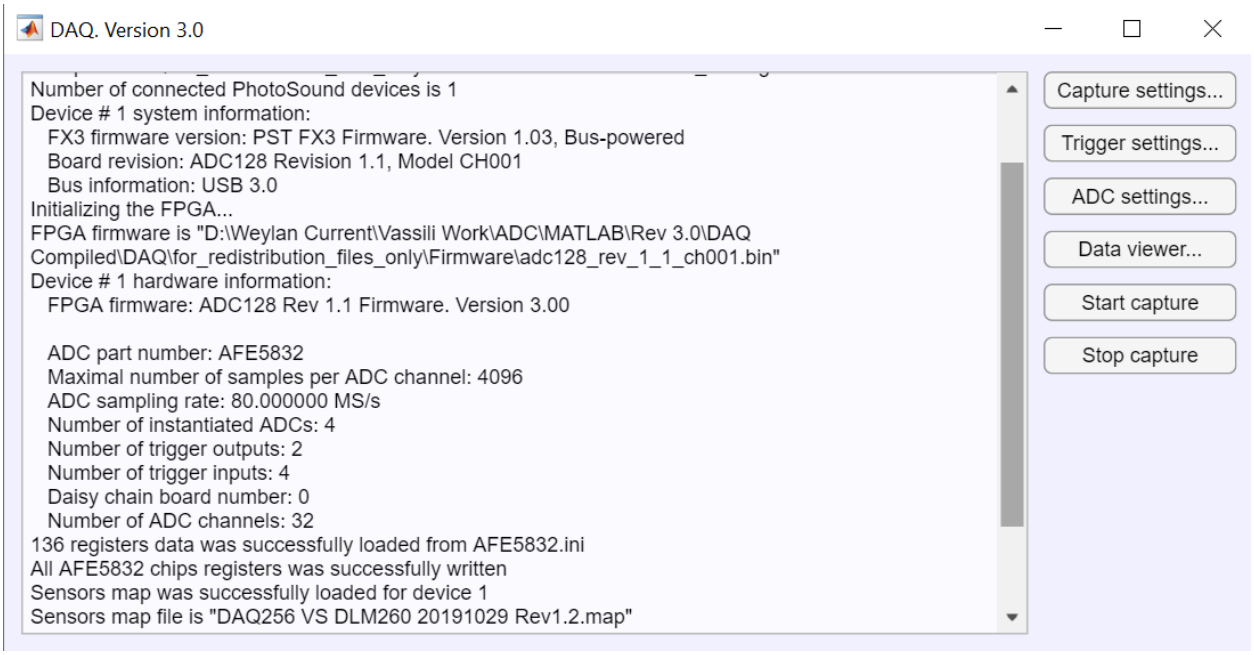

Figure 9: After starting the software, wait until the firmware version is displayed and 'All AFE5832 chips registers were successfully loaded' before starting the session.

Wait until the firmware version is displayed before starting the session. The loading of firmware might take about 45 seconds. If the session is started before all AFE5832 chips are loaded, the session might be unresponsive or act with delay. If the session is unresponsive or problematic, restart it by ending the DAQ.exe program from the task manager.

The DAQ.exe program will all windows open is shown in Figure 10.

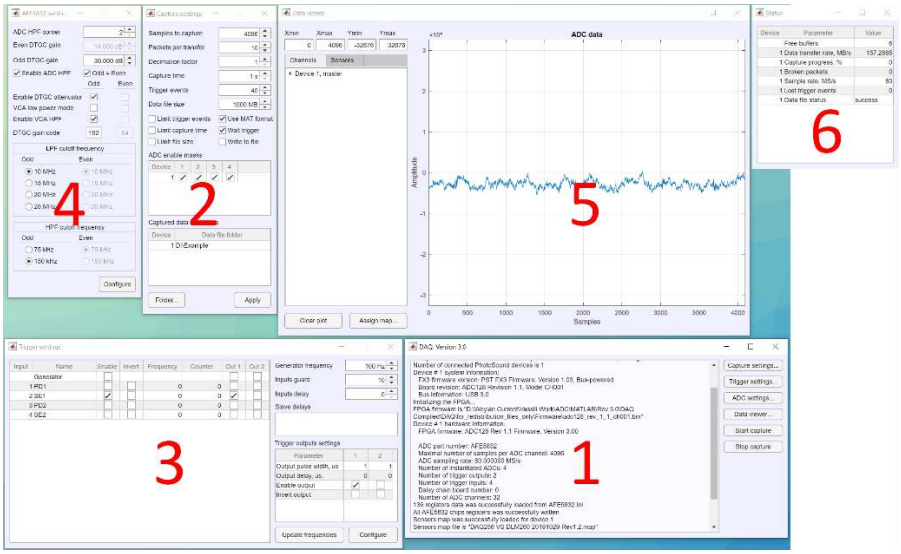

Figure 10: After firmware is loaded, configure the trigger and sampling parameters of ADC128.

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PhotoSound Data Acquisition Application Window Guide

This section will familiarize the user with the DAQ application's multiple windows.

DAQ Window

The DAQ Window (Figure 11) is the main hub of the DAQ.exe application. When the DAQ.exe application is started, only the DAQ Window will appear.

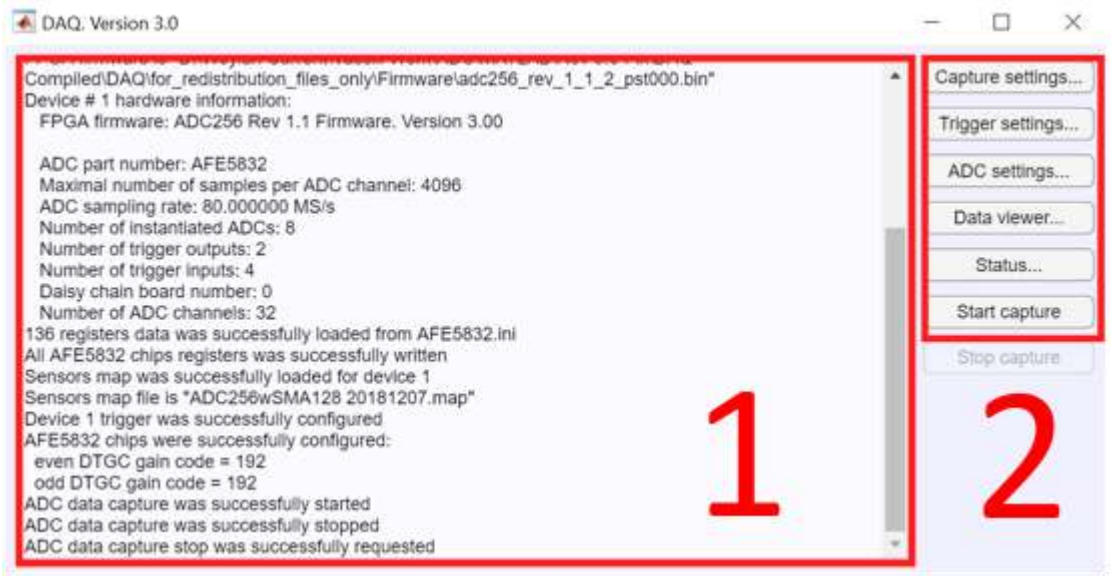

Figure 11: DAQ Window

The DAQ Window has two sections: the log (1) and the control buttons (2).

1. The log (1) shows an updating readout of all actions taken by the DAQ.exe application.
2. The control buttons (2) are used to open other windows of the application and to command the start and stop capture of the DAQ board.
   a. The 'Capture settings' button will open the Capture Window.
   b. The 'Trigger settings' button will open the Trigger Window.
   c. The 'ADC settings' button will open the ADC Window.
   d. The 'Data viewer' button will open the Data Window.
   e. The 'Status' button will open the Status Window.
   f. The 'Start capture' button will start the acquisition of data.
   g. The 'Stop capture' button will stop the acquisition of data.

Capture Window

The Capture Window (Figure 12) has three sections: the capture settings (1), the enable ADC setting (2), and the save directory (3).

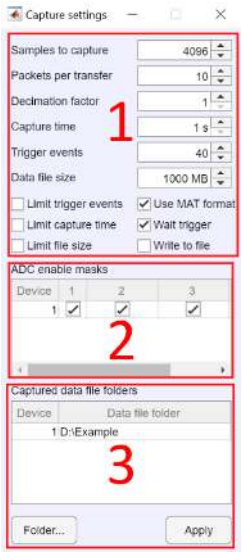

Figure 12: Capture Window

1. The capture settings (1) allow the user to change the data acquisition parameters.
    - Samples to capture – a value that is defined by the maximum resolution of the DAQ boards, 12-bit. The maximum value, 4096, can be lowered at the will of the user. Changing this parameter will set the data acquisition board to record the number of samples specified. Note: The sampling rate of the ADC boards is 80 MHz (40 MHz from each lane of the ADC chips).
    - Packets per transfer – indicates how many frames will be in a transfer event through the USB 3.0 connection. PST recommends a value between 5-10 for 100-200 Hz triggers. Increase the packets per transfer only if there are lost trigger events.
    - Decimation factor – down samples the fixed 80 MHz sampling rate of the ADC boards by the factor specified. Note: This does not physically change the sampling rate of the ADC boards but instead drops the sampling events in the memory buffer needed to reach the specified down sampled sampling rate. The dropped events are equally temporally spaced.
    - Capture time – Limits the amount of time the DAQ will acquire data, measured in seconds.
    - Trigger events – Limits the amount of trigger events the DAQ will acquire data for.
    - Data file size – Limits the size of the final acquired data that the DAQ will trigger for.
    - Limit trigger events – enables the limit trigger events setting that will stop data acquisition when the value of 'Trigger events' is reached.
    - Limit capture time – enables the limit capture time setting that will stop data acquisition when the value of 'Capture time' is reached.
    - Limit file size – enables the limit file size setting that will stop data acquisition when the final acquired file size exceeds the value of 'Data file size'.

- Use MAT format – when enabled, formats the acquired data as a mat file. When disabled, formats the acquired data as a binary bat file.
- Wait trigger – enables the ADC setting that waits for a user defined trigger input (the internal generator is also defined as a trigger input). Left unchecked, the ADC board will acquire data at the maximum possible frequency that will result in no lost packets regardless of trigger inputs.
- Write to file – enables the setting of writing data to the solid-state drive. Left unchecked, no data acquired by the ADC will be written to the SSD.

2. The enable ADC setting (2) allows the user to select which ADC chips will acquire data. There are four ADC chips in the DAQ128 and eight ADC chips in the DAQ256. The table lists entries by device in the case that multiple devices are linked in a master-slave configuration.
3. The save directory (3) allows the user to change the output file location that the acquired data will be saved to. Select the device number in the table and click the 'Folder' button to bring up a UI dialog to navigate to the output directory.

The 'Apply' button in the save directory (3) section applies all of the settings in the Capture Window. None of the settings will be updated until the 'Start capture' button is next pressed in the DAQ Window (Figure 11).

MATLAB File Metadata

The *.tdms to *.mat conversion conserves the *.tdms header metadata. The *.mat file has the following metadata headers:

- data_# - The '#' in the 'data_#' array is the frame number of the recorded data. The dimensions of the 'data_#' array are Channel number x Channel Samples x ADC Chip.
- adc_mask – described enabled or disabled state of 8x 32-channel ADC-chips which translates the data. If all ADC chips are enabled, the mask is $_{d}255 = {}_{b}11111111$.
- board_number – This array is only relevant if two or more ADC boards are linked in a Master-Slave configuration. The variable distinguishes which 'data_#' was recorded on each ADC board.
- packet_number – This array records the packet number of each 'data_#' frame. The 'packet_number' starts at 0 when the ADC is turned on and continuously updates upon being triggered.
- sample_rate – states the sampling rate of the DAQ boards. With a decimation factor of 1, the sampling rate is 40 MHz.
- trigger_source – an array that lists the trigger source of each frame acquired by the trigger input ID listed in the Trigger Settings dialog.
- trigger_time – an array that lists the time each frame was triggered in ms. The timing starts from the first acquisition event after the board is powered. The timing only increases when the board is actively acquiring data.

Trigger Window

WARNING: The SMA (SE1/SE2) trigger inputs can only accept a specific pulse trigger as shown in Figure 13.

- The frequency of this pulse can be between (0,240] Hz.
- The pulse width must be small; maximum 5% duty cycle, ideally 1% duty cycle.
- Rising/falling edge can be minimum allowed setting.
- The voltage MUST be from [0, 5] V. A value lower than 5 V can be used as the maximum, but in practice anything below 4 V will not trigger the SMA input.

The middle graph shows a bad SMA trigger input. The input has a negative voltage component. This is not allowed.

The bottom graph shows a bad SMA trigger input. The input has a duty cycle above 5%. This will eventually burn the SMA impedance resistor.

By default the input impedance of the SMA triggers are 50 Ohm. Removing the J13 jumper will make the SMA trigger input (I0) impedance HiZ. Removing the J16 jumper will make the SMA trigger input (I1) impedance HiZ. Make sure that the triggering device's output impedance load matches the input impedance setting of the DAQ128.

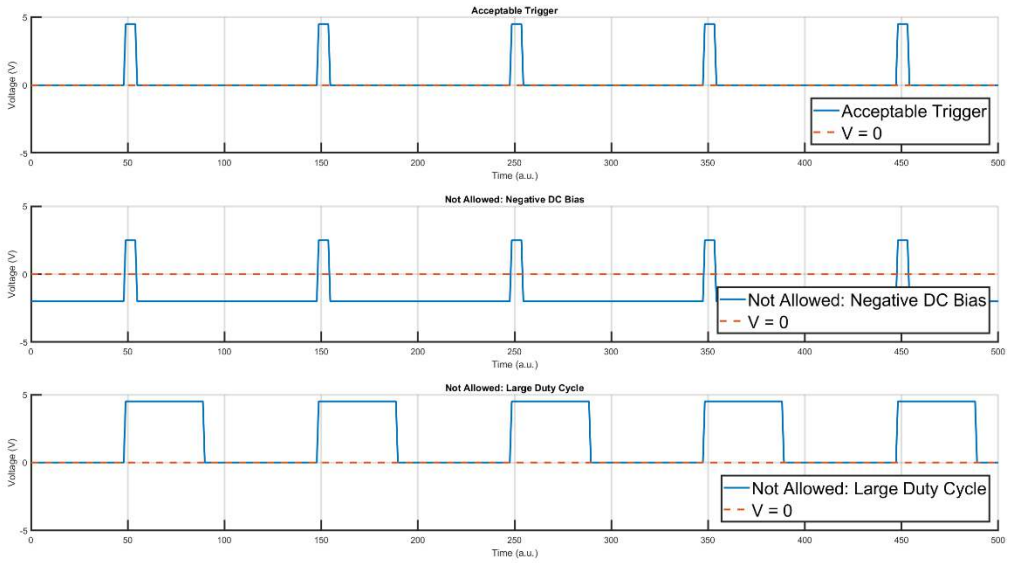

Figure 13: Trigger Input Pulse Acceptance. SMA trigger IO (signal and input ground) are electrically isolated with respect to the rest of ADC circuitry. SMA IN1 trigger input and OUT1 trigger output share the ground level. SMA IN2 trigger input and OUT2 trigger output share the ground level, which is different from the ground for SMA IN1 and OUT2. The trigger level (blue line) is measured with respect to the trigger coaxial cable shield (level 0). The trigger large duty cycle shown on the last graph is acceptable with HiZ trigger input termination, which can be delivered upon request or require disassembly of ADC, removal of PCBs and removal of the jumpers J13 and/or J16 used to set the trigger input impedance.

The Trigger Window (Figure 14) has three sections: the trigger selection (1), the generator and delay (2), and the trigger output settings (3).

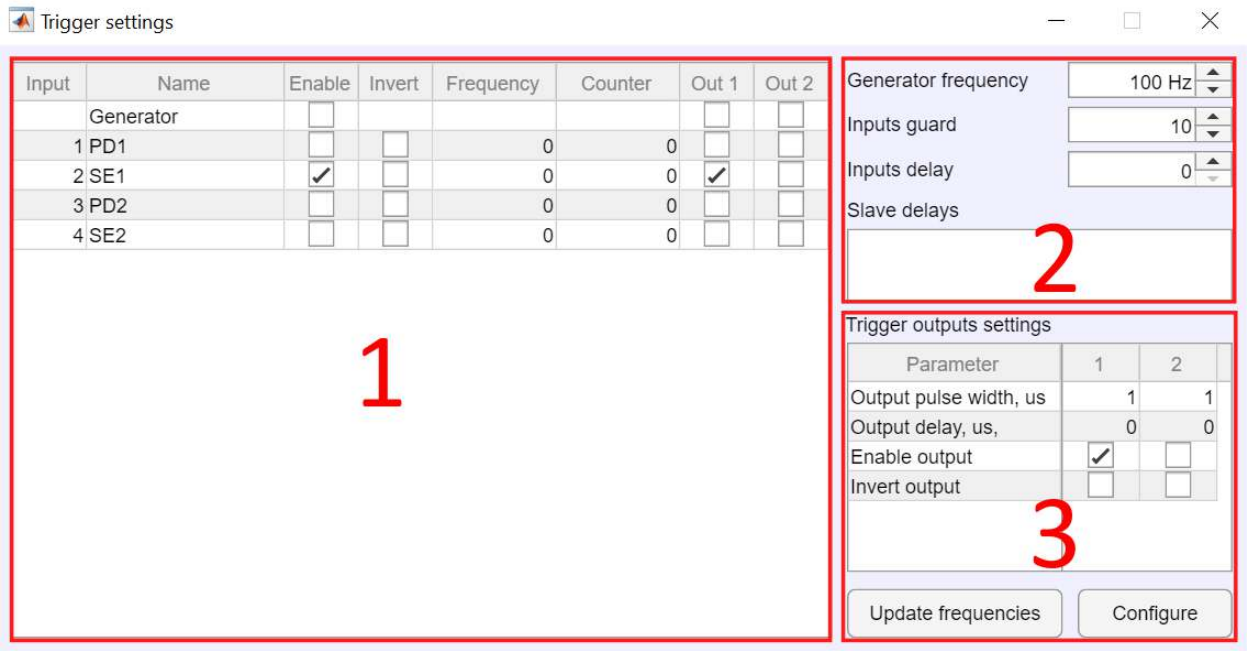

Figure 14: Trigger Window

1. The trigger selection table (1) selects the trigger input and output sources as well as lists the triggering options of the DAQ board.
    - Inputs
        i. Generator – Internal generator of the DAQ board. The frequency of the generator is set in the generator and delay section (2).
        ii. PD1 – Photodiode input 1, 'PD1' on the external label of the board.
        iii. SE1 – SMA Electric input 1, 'I1' on the external label of the board.
        iv. PD2 – Photodiode input 2, 'PD2' on the external label of the board.
        v. SE2 – SMA Electric input2, 'I2' on the external label of the board.
    - Enable – enable checkbox for each trigger input allows the device to be triggered by the enabled inputs. Multiple inputs can be enabled at the same time.
    - Invert – enables the inversion of the trigger output signals.
    - Frequency – displays the frequency of the acquired trigger. This will update only when the device is not capturing data and the 'Update frequencies' button is pressed.
    - Counter – counts the number of recorded trigger events. This will update only when the device is not capturing data and the 'Update frequencies' button is pressed.
    - Out 1 – checkbox enables the trigger input signal to be sent to the trigger output 1 of the board, 'O1' on the external label of the board. Note: this will not enable the trigger output 1 of the board, send the trigger input(s) selected to the trigger output 1.
    - Out 2 – checkbox enables the trigger input signal to be sent to the trigger output 1 of the board, 'O2' on the external label of the board. Note: this will not enable the trigger output 1 of the board, send the trigger input(s) selected to the trigger output 2.
2. The generator and delay section allows the user to change the internal generator frequency and delays of the trigger and slave boards.
    - Generator Frequency – sets the internal generator frequency in Hz.

- Inputs Guard - rejects trigger inputs at the start of data acquisition for the specified ADC clock counts. This prevents erroneous trigger input detection when an acquisition starts. (Recommended value is 10 clock cycles).
- Inputs delay – delay between the registration of the trigger and start of data recording. The value is calculated in ADC clock counts.
- Slave delays – delay between a trigger even of the master board to the slave board, measured in ADC clock counts. The PST recommended settings for slave delays of multiple boards is [(Slave1, 5),(Slave2, 7), (Slave3, 9)]. In practice, these slave delays fluctuate upon startup of multi-board DAQ systems, but will generally be in the range stated above.

3. Trigger output settings (3) enables the configuration of the trigger outputs. Column 1 refers to trigger output 1 (O1) and column 2 refers to trigger output 2 (O2).
    - Output pulse width, us – set the pulse width of the trigger output in µs.
    - Output delay, us – sets the delay between the trigger input signal and trigger output signal in us.
    - Enable output – checkbox enables the trigger output of the board. The trigger output signal is defined by the selection of checkboxes in the trigger selection table (1).
    - Invert output – checkbox enables the trigger output of the board to be inverted. The selection of trigger output inverted signals is defined by the selection of checkboxes in the trigger selection table (1). An example inverted output is shown in (Figure 15).

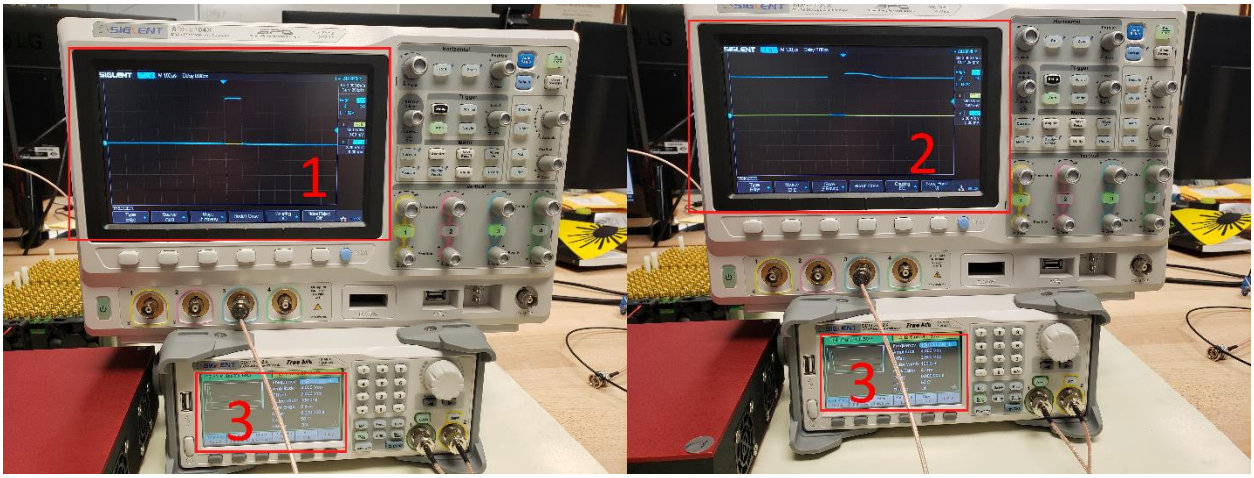

Figure 15: Inverted trigger output. The non-inverted trigger output (1) compared to the inverted trigger output (2). The same input pulse signal (3) is fed to the output.

The update frequency button will update the trigger selection table's (1) Frequency and Counter columns.

NOTE: The 'Configure' button must be pressed for the chosen setting to be sent to the DAQ board. This button can be pressed at any time, regardless of whether the DAQ is capturing data or idle. Pressing the 'Configure' button during acquisition might result in a few lost frames.

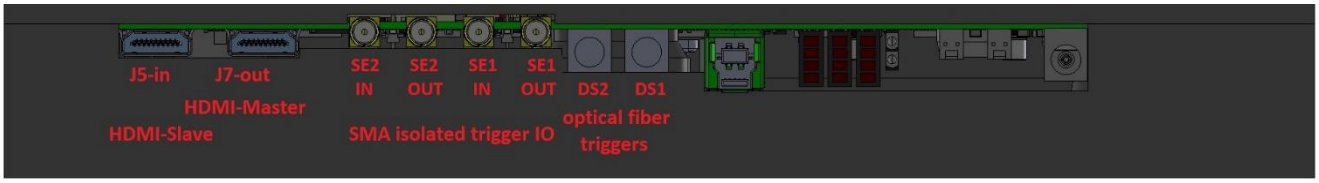

Figure 16: ADC256 front panel connectors labeled according to Input source selection. AMP128 boards are not shown.

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ADC Window

The ADC Window (Figure 17) has three sections: main control section (1), LPF section (2), HPF section (3), and ADC selection (4). Note: There are two ADC chip settings on the DAQ window. 'AFE5832 settings' is used for LEGION DAQ128/256 products. 'AFE5818 settings' is used for FLASH DAQ32 products.

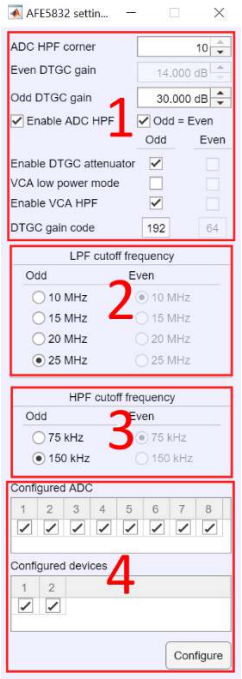

Figure 17: ADC Window

1. The main control section (1) allows the user to modify settings that directly interface with the TI AFE5832 ADC chips on the DAQ PCB.
    - ADC HPF corner – switches the high pass filter options on the AFE5832 chip that is described in Figure 18. Note: Figure 18 is the HPF corner plot for the AFE5851 chip, the AFE5832 chip has very similar values for the HPF corner settings.
    - Even DTGC gain – sets the Digital Time Gain Compensation of the even channels on the DAQ256 boards in dB.
    - Odd DTGC gain – sets the Digital Time Gain Compensation of the odd channels on the DAQ256 boards in dB.
    - Enable ADC HPF – checkbox enables the DAQ256 high pass filter
    - Odd = Even – checkbox enables the odd and even channels of the DAQ256 boards to act identically and disables the Even options in ADC Window.
    - Enable DTGC attenuator – checkbox enables the Digital Time Gain Compensation attenuator, use this if you have set the DTGC gain values to the minimum and still have saturated data acquisition signals.
    - VCA low power mode – enables the low power mode of the Voltage-Controlled Amplifier. This modifies the gain and bandwidth ranges of the ADC chips.
    - Enable VCA HPF – enables the high pass filter of the voltage-controlled amplifier.

- DTGC gain code – outputs the DTGC gain code of the set Even/Odd DTGC gain. The gain codes are shown in Figure 18.

2. The LPF cutoff frequency module (2) sets the low-pass filter cutoff frequency of the ADC chips. A selection of four frequencies are listed with radio buttons for both even and odd channels.
3. The HPF cutoff frequency module (3) set the high-pass filter cutoff frequency of the ADC chips. A selection of two frequencies are listed with radio buttons for both even and odd channels.
4. The ADC selection section (4) allows the user to choose which ADC chips or Devices will be affected by the configured ADC Settings.

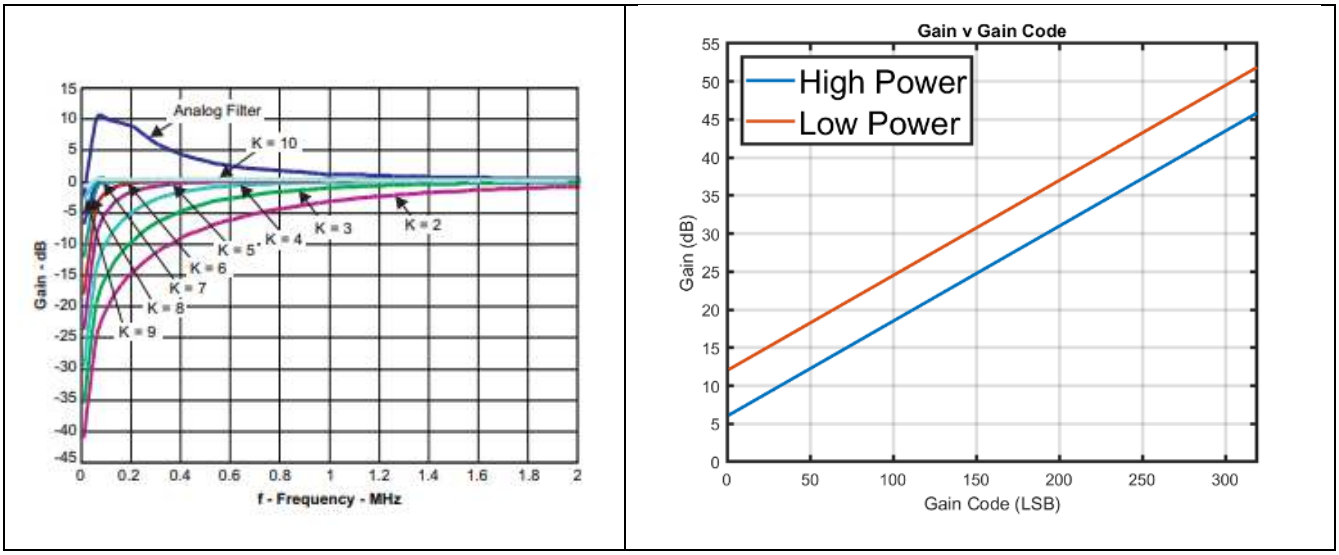

Figure 18: AFE5851 HPF Corner (Left) and DTGC gain codes (Right)

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Data Window

The Data Window (Figure 19) has two sections: the channel table (1) and the oscilloscope (2).

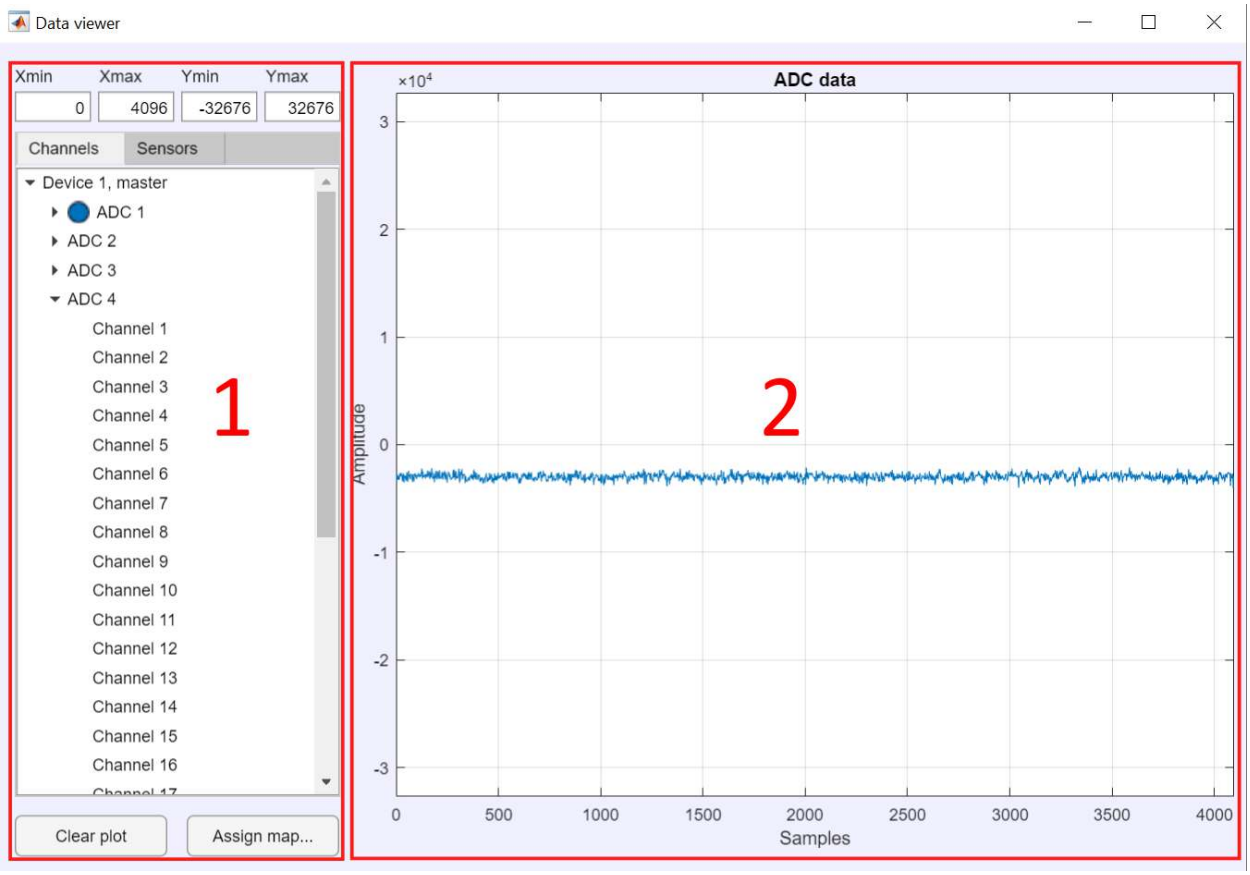

Figure 19: Data Window

1. The Channel/Sensors selection boxes allow a user to visualize any or all of the channels of data acquired from the DAQ boards.
    - Textboxes at the top (1) allow the user to set the boundaries of the virtual oscilloscope (2) at the top where the 'X' dimension is Channel Samples and the 'Y' dimension is a signed 16-bit digitalization of the ADC boards' voltage range of 2 Vpp.
    - The channel tab of dialog box in the center lists the two DAQ boards as Device 1 and Device 2, this assignment of devices is dependent on the order that the attached computer's motherboard assigns the two DAQ boards. The designator of 'master' and 'slave' are tied to the physical configuration of the HDMI cable connecting the two boards.
    - Clicking on the dropdown arrow next to a Device will show the number of ADC chips, of which there are four/eight per Device (DAQ128/DAQ256).
    - Each ADC also has a dropdown arrow next to it that will list the channels per ADC chip, which is 32-channels per ADC chip. Selecting either a channel, ADC chip, or Device will plot the chosen selection onto the virtual oscilloscope (2). To clear all visualized channels, click on the 'Clear plot' button at the bottom.
    - The dialog box has a second tab called the 'Sensors' tab. The ADC boards do not arrange the channels that are interfaced between the probe and amp connectors; therefore, a

channel mapping must be applied to correctly arrange the channels. The channel map is included in the directory of the DAQ.exe application or a custom channel map can be applied by selecting the 'Assign map…' button AFTER selecting a device in the Sensors list.

- Once a selected map is assigned, the Sensors tab will populate with arranged channels from the Channels tab. The Sensors tab will be arranged as (Sensor 1, Sensor 2, …, Sensor 256) by Device (Figure 20). Each 'Sensor #' will also have the original ADC chip and Channel beside the entry as (A#C#) where 'A#' is the ADC chip number and 'C#' is the channel number.

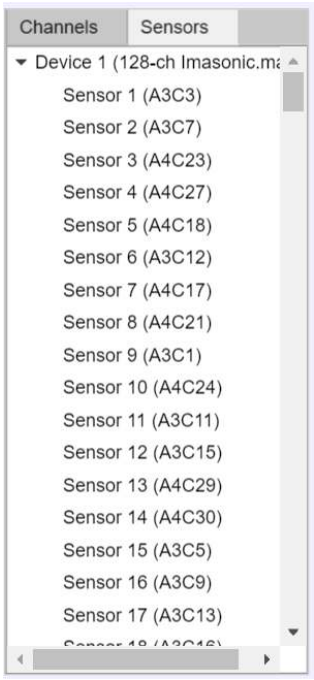

Figure 20: Sensors Selection Box

2. The virtual oscilloscope (2) shows the readout of the acquired data frame. The plot will only visualize selected channels from the Channels/Sensors tab (1). The colors of each channel's signals are assigned cyclically over seven colors in the Channels/Sensors tab (1) upon selection; to change colors of a signal, unselect then select the same channel. The x-axis of the plot shows the number of Samples captured while the y-axis of the plot shows the signed 16-bit digitalization of the ADC boards captured voltage range of 2 Vpp. Signals exceeding the limits of a signed 16-bit converted voltage are considered to be oversaturated. The visualized data updates at 10 Hz.

Status Window

The Status Window has one section that displays the status of data acquisition.

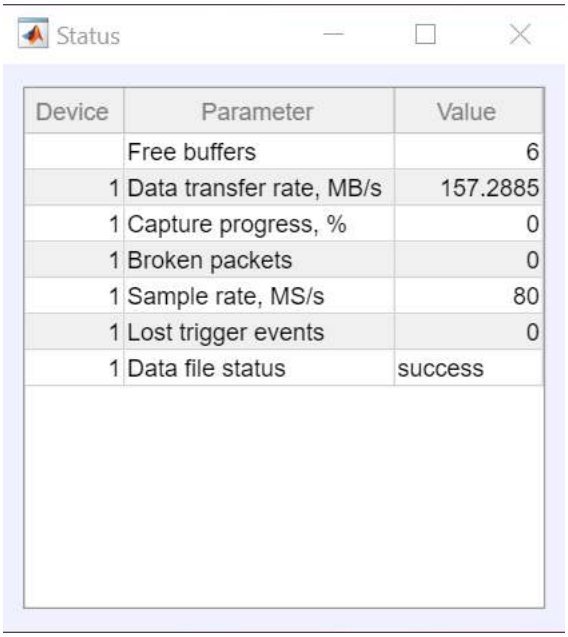

Figure 21: Status Window

- Data transfer rate, MB/s – displays the data transfer rate through the USB3.0 cable.
- Capture progress, % - if using a limit triggers/time/size checkbox in the Capture Window, this displays the percentage of the process that is completed.
- Broken packets – shows the number of broken packets since the last 'Start capture'.
- Sample rate, MS/s – shows the sampling rate of the DAQ board, will update based on the chosen decimation factor.
- Lost trigger event – displays the number of lost triggers since the last 'Start capture'.
- Data file status – displays the status of the capture event.

DAQ Examples

The DAQ boards have some unobvious behavior with the signals. A couple of test cases will be detailed below:

1. Even-odd channel delay. Figure 22, which shows the effect in a different software (LabVIEW), shows the effect of the even/odd channel delay during data acquisition of the DAQ board. The odd signals lag behind the even signals by 1 ADC clock cycle = 12.5 ns.

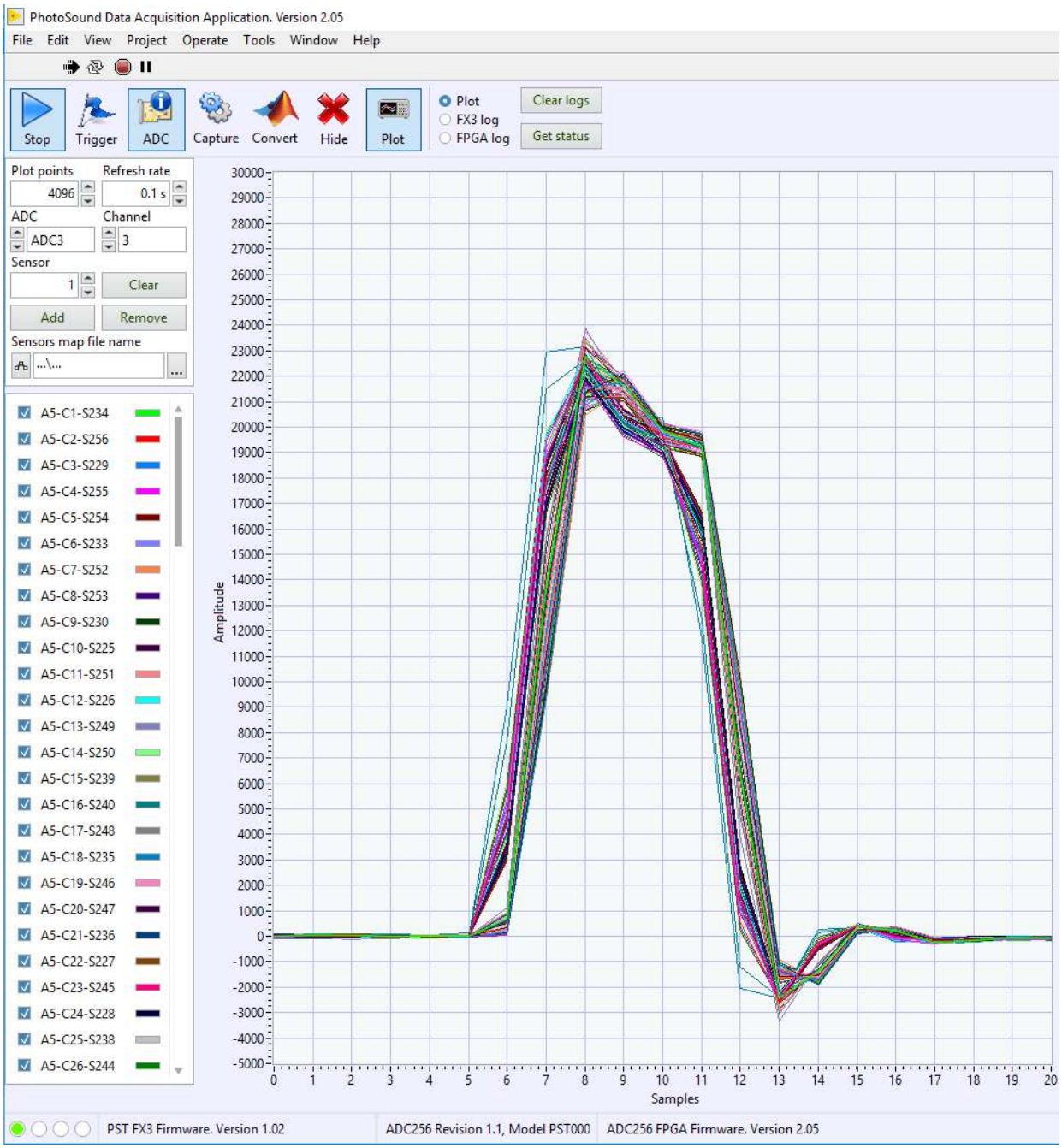

Figure 22: Trigger output SE was looped back through 20 dB attenuator to all 128 channels of ADC5 – ADC8. Odd signals lags behind even channels by ½ sample = 1 ADC clock = 12.5 ns. The signal is steady: the jitter between frames in this regime is much less than ADC clock rate.

2. HPF enabling. Figure 23 shows the effect of enabling the HPF, which removes any DC bias from the acquired data.

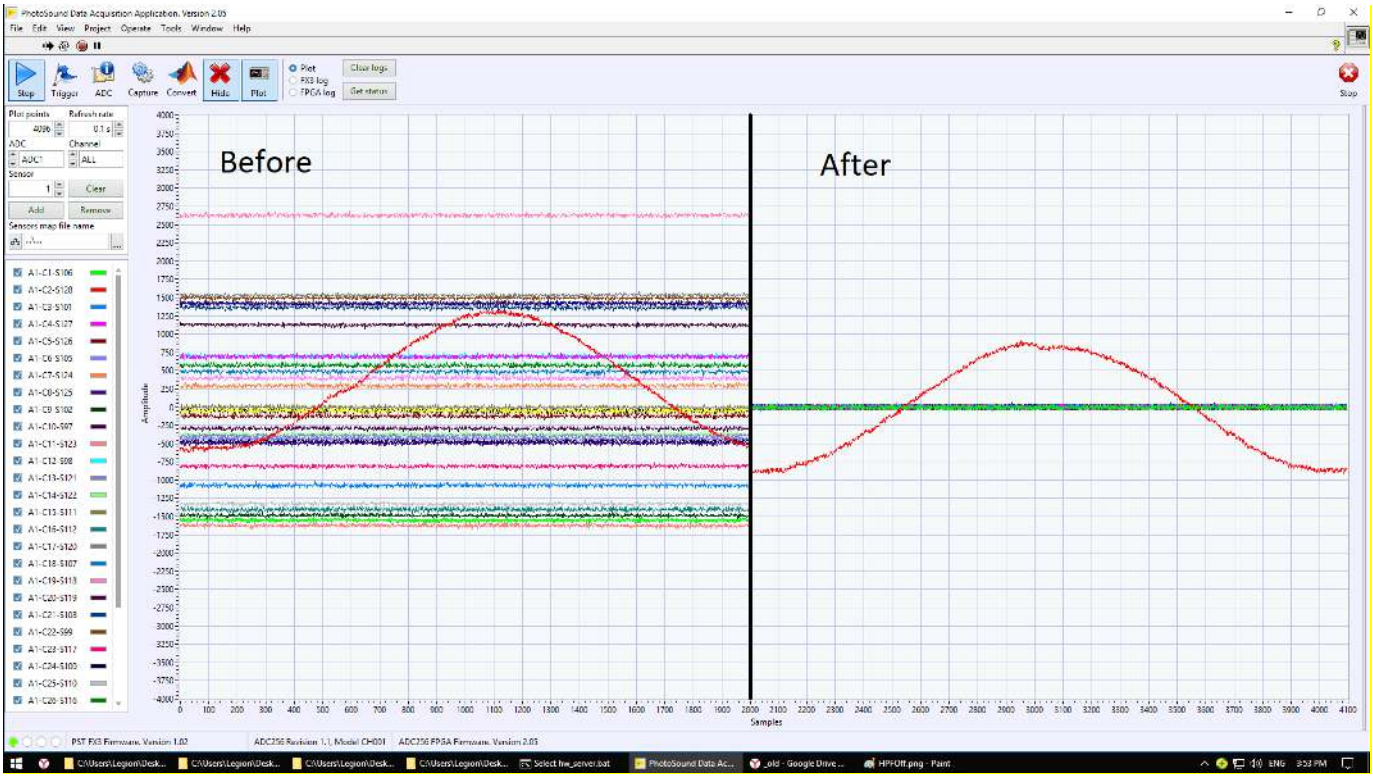

Figure 23: High Pass Filter settings. Before waveforms are visualized with no HPF applied. After waveforms are visualized with HPF corner = 10 for all ADCs. Notice removal of DC bias effect.

Multiple ADC boards configuration

Use HDMI interface for multiple ADC boards configurations only. Use standard HDMI cables, but **do not connect a monitor or video source to HDMA connectors on ADC board**. For ADC256 Rev1.1 choose any board as master (MS), use the other board(s) as slave(s). Connect HDMI cable to J5-in on slave board and J7-out on master board. If more than 2 ADC boards are used, use the fist slave as a master for the second slave, and the second slave as a master for the third slave. Master board and slave board(s) will be recognized and sorted automatically according they position in daisy chain. If more than 4 boards are used in parallel or minimal dead time (zero or negative) required for the board configuration, a special trigger and clock server (under development) can be used to trigger and control the boards.

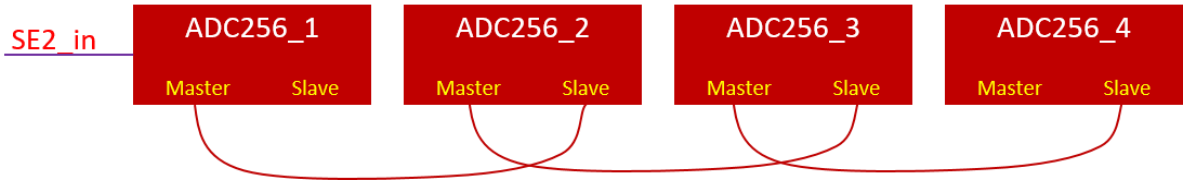

Figure 24: Principal schematics of connection of 4 ADC256 boards as daisy chain using 3 HDMI cables (red). Trigger must be supplied to the first master board (ADC256_1) like in a single board configuration.

- Any ADC256 R1.1 and higher can serve as a master or slave board. The master and slaves are found dynamically according to HDMI cable configuration.
- Run one run one copy of software for all boards:
  - The ADC chips and channels are counted starting from the first master board.
  - The slave boards are represented as extra ADC chips on the master ADC board.
  - Recognized ADC boards are first shown as yellow indicator in the status line of DAQ.exe
- The program is fully initiated after all round indicator in the status line of ADC.exe/vi software turned green from yellow.
- Verify LEDs after program is started and ADCs are fully initiated
  - The first master ADC: 2 green LEDs on LD2 (LED column next to USB3 connector),
  - All slave ADCs: all 4 green LEDs on LD2.
- Verify trigger synchronization between the boards.
  - In the trigger menu, first choose generator as a trigger input source. Reduce the trigger rate as needed, for example 400000 for 20 Hz.
  - Monitor waveforms from all ADC boards, for example ADC1, ADC9, ADC17, ADC25 for 4 ADC board configuration.
- The external trigger should be applied to the first master board only. Configure the trigger for the first master board like the trigger for the only ADC board.